

UNITED STATES PATENT APPLICATION

of

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for

**ELECTRONIC SYSTEM MODELING USING ACTUAL AND APPROXIMATED
SYSTEM PROPERTIES**

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ELECTRONIC SYSTEM MODELING USING ACTUAL AND APPROXIMATED SYSTEM PROPERTIES

BACKGROUND OF THE INVENTION

Cross-Reference To Related Applications

5 The subject application is related to the following copending applications:

U.S. Patent Application Serial No. 09/106,478 (~~Atty. Docket No. 112025-0077~~),
filed June 29, 1998, entitled "PROGRAMMABLE ARRAYED PROCESSING ENGINE
ARCHITECTURE FOR A NETWORK SWITCH";

U.S. Patent Application Serial No. 09/106,436 (~~Atty. Docket No. 112025-0079~~)
10 entitled, "ARCHITECTURE FOR A PROCESSOR COMPLEX OF AN ARRAYED
PIPELINED PROCESSING ENGINE," filed June 29, 1998;

U.S. Patent Application Serial No. 09/106,244 (~~Atty. Docket No. 112025-83~~), en-
titled, "SYSTEM FOR CONTEXT SWITCHING BETWEEN PROCESSING
ELEMENTS IN A PIPELINE OF PROCESSING ELEMENTS," filed June 29, 1998;

U.S. Patent Application Serial No. 09/106,246 (~~Atty. Docket No. 112025-0084~~)
15 entitled, "SYNCHRONIZATION AND CONTROL SYSTEM FOR AN ARRAYED
PROCESSING ENGINE," filed June 29, 1998;

U.S. Patent Application Serial No. 09/213,291 (~~Atty. Docket No. 112025-0085~~),
entitled "PARALLEL PROCESSOR WITH DEBUG CAPABILITY," filed December
20 14, 1999;

U.S. Patent Application Serial No. 09/216,519 (~~Atty. Docket No. 112025-112~~), en-
titled "TIGHTLY COUPLED SOFTWARE PROTOCOL DECODE WITH
HARDWARE DATA ENCRYPTION," filed December 18, 1998; and

U.S. Patent Application Serial No. 09/212,314 (~~Atty. Docket No. 112025-118~~) en-
titled "TESTING OF REPLICATED COMPONENTS OF ELECTRONIC DEVICE,"
filed December 14, 1998.

Each of the aforesaid copending applications is assigned to the Assignee of the
subject application, and is incorporated herein by reference in its entirety.

Field of the Invention

The present invention generally relates to computer modeling of electronic sys-
tems, and more specifically, to a computerized electronic system modeling and simula-
tion technique that uses both actual and approximated/estimated properties of the system.
Although the present invention will be described in connection with computer aided
modeling of a portion of a parallel processor, other utilities are also contemplated for the
present invention, including modeling of other types of electronic systems, and features
and components thereof, and in other types of computer aided design applications.

Brief Description of Related Prior Art

Typically, during the process of formulating and validating a proposed electronic
system design, it has been desirable to use computer aided design (CAD) techniques to
model and simulate the operation of the proposed design, prior to physically fabricating
the proposed system. By employing such modeling and simulation techniques, it is often
possible to determine whether potential problems (i.e., design faults) are present in the
proposed design, and if necessary, to modify the proposed design to reduce or eliminate

such potential problems, without ever physically constructing and testing the system being designed. Thus, by employing such modeling and simulation techniques, the cost and time required to validate a proposed design may be significantly reduced.

However, it has been found that in order to meaningfully model and simulate the operation of certain systems, special considerations must be taken into account. For example, a high speed, high performance parallel processor includes a significant amount of high speed, sequential logic and other clocked circuitry whose proper operation often is critical to proper performance of the parallel processor. Therefore, at most, only minor timing faults in such circuitry can be permitted, if the system is to function acceptably. Thus, in order to meaningfully simulate the operation of a proposed parallel processor design, the timed operation of the parallel processor's clocked circuitry must be simulated with a high degree of accuracy. This need is particularly acute with respect to timing operations involving parallel processor circuit modules that are interconnected by intermodule network connections, as such network connections typically exhibit a relatively large amount of impedance and capacitance that may introduce significant propagation delays into signals traversing the network. This necessitates that the CAD system be able to determine very accurately the propagation delays of such signals.

One conventional CAD simulation technique that is able to accurately determine the propagation delay of a signal through a circuit network calculates the delay based upon the actual physical characteristics (e.g., characteristic impedances, capacitances, etc.) of the branches of the network through which the signal propagates, as well as, the actual physical characteristics of the transmitter (e.g., output impedance, charging capacitance, etc.) and intended receiver (e.g., input impedance, charging capacitance, etc.)

of the signal. These actual physical characteristics may be calculated by the CAD system based upon physical design data that describe physical features of the proposed design such as the physical layout of the design's circuit paths, the physical properties of the active and passive electronic components interconnected by those paths, etc., and well
5 known physical laws that correlate these and other features of the proposed design to the physical characteristics to be calculated.

Unfortunately, in practice, it is often difficult or impossible to employ this conventional technique to simulate the operation of certain highly complex parallel processor designs (such as those described in the aforesaid copending applications). This is be-
10 cause, in practice, the amount of computer processing time (hereinafter termed "processing overhead") required to accurately simulate the operation of such highly complex designs using such physical characteristics often is extremely large, and in extreme cases, can be prohibitive.

One proposed solution to this problem involves using so-called "hierarchical
15 analysis" (HA) techniques. In HA, rather than basing the simulation of the design's timing operation upon the design's actual physical characteristics, the simulation is instead based upon approximate or estimated mathematical models of operation of portions of the design. That is, respective mathematical models are generated for respective functional blocks comprising the design which may be used to estimate the timing operation of the
20 design. The design's timing operation is then simulated using these approximate models.

Unfortunately, although HA is able to reduce the amount of processing overhead needed to simulate a design's timing operation, it inherently introduces approximation error into such simulation. This causes timing operation simulations that are based solely

upon HA-models to be inherently less accurate than timing operation simulations based upon actual physical characteristics.

5 This inherent inaccuracy of HA-based simulations results in certain disadvantages. For example, in order to try to ensure that the simulation uncovers all potential timing faults in the design, it may be necessary to adjust the simulation such that it is based upon worst case (i.e., most pessimistic) calculations of signal propagation delays in the design. Unfortunately, when "worst case analysis" is used, a sizable number of the timing faults identified by the simulation may actually be erroneous. This erroneous identification of timing faults may introduce significant inefficiencies into the design process. For example, a designer encountering an erroneous timing fault may believe that the fault actually is present in the design, and therefore, may unnecessarily modify the design to correct the supposed fault. This may unnecessarily increase the time and expense required to formulate and validate the design.

SUMMARY OF THE INVENTION

15 In accordance with the present invention, an electronic system modeling technique is provided that overcomes the aforesaid and other disadvantages and drawbacks of the prior art. In broad concept, the technique of the present invention bases the simulation of the operation (e.g., timing operation) of a proposed electronic system design upon both actual physical characteristics of a portion of the design, and HA-based approximate models of the rest of the design. The portion of the design that is modeled using its actual physical characteristics may be selected so as to reduce error in the simulation to

below a minimum desired threshold without increasing the amount of processing overhead needed to generate the simulation to an undesirable level.

Advantageously, when an electronic system design is modeled and its operation is simulated in accordance with the present invention, the resulting simulation may be substantially more accurate than when the design is modeled and its operation is simulated solely in accordance with conventional HA techniques. Indeed, the resulting simulation in accordance with the present invention may be sufficiently accurate to make the need to use the above-discussed type of worse case analysis unnecessary. Additionally, the amount of processing overhead required to simulate the design's operation in accordance with the present invention may be only slightly more than that required to simulate the design's operation using only conventional HA models of the design.

The aforesaid and other features and advantages of the present invention will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, wherein like numerals depict like parts, and in which:

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a highly schematic, functional block diagram of a modeling and simulation system wherein one embodiment of the present invention is advantageously practiced.

Figure 2 is a highly schematic, functional block diagram of the physical characteristic modeling engine in the system of Figure 1.

Figure 3 is a highly schematic block diagram of an electronic system design that the system of Figure 1 may be used to model.

Figure 4 is a highly schematic block diagram illustrating modeling of the design of Figure 3 according to a conventional HA technique.

Figure 5 is a highly schematic block diagram illustrating modeling of the electronic system of Figure 3 in accordance with one embodiment of the present invention.

5 Figure 6 is a highly schematic, functional block diagram of a conventional HA modeling and simulation system.

As will be appreciated by those skilled in the art, although the following Detailed Description will proceed with reference being made to specific embodiments and methods of use, the present invention is not intended to be limited to these embodiment and methods of use. Rather, the present invention is intended to be viewed broadly as encompassing all alternatives, modifications, and variations from these embodiments and methods of use as are included within the spirit and broad scope of the hereinafter appended claims.

15 **DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS**

Figure 1 illustrates a system 10 wherein one embodiment of the technique of the present invention for modeling and simulating timing operation of a proposed electronic system design 100 is advantageously practiced. Figure 6 illustrates a conventional system 300 for modeling and simulating timing operation of design 100 using only conventional HA models. Although not shown in the Figures, systems 10 and 300 each comprise computer-readable memory (e.g., random access, read only and/or mass storage computer memory) for storing software programs and associated data structures for exe-

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cution by one or more processors also comprised in the respective systems 10, 300. When executed by the one or more processors respectively comprised in systems 10, 300, the software programs and data structures cause the respective systems 10, 300 to carry out and/or implement the respective techniques, functions, and operations described herein as being carried out and/or implemented by the respective systems 10, 300 and their respective functional blocks (i.e., blocks 20, 22, 24, 26, 28, 30, 32 in system 10, and blocks 20, 22, 24', 26, 28, and 32' in system 300, respectively). As will be apparent to those skilled in the art, many types of computer processors and memories may be used in system 10 without departing from the present invention.

10 By way of example, for purposes of illustrating the operation of the system 10, and with reference being made to Figure 3, the proposed design 100 may be part of a parallel processor system of the type described in the aforesaid copending patent applications, and may include a plurality of functional modules or blocks (i.e., function blocks A, B, C, D, X, Y, and Z) 60, 62, 64, 66, 72, 74, 76 that interact with each other and generate outputs 78 based upon inputs 50, 80 and timing (i.e., clock) signals CLK. The 15 blocks 60, 62, 64, and 66 may together comprise one logical circuit module 65 that produces outputs, and transmits the outputs via electrical connection (e.g., intermodule connection) 70 to another logical circuit module 67 comprising blocks 72, 74, 76. The module 67 may use the outputs provided to it from the module 65 to generate output signals 20 that are supplied to other circuit elements (not shown) external to the design 100.

By way of illustration, the circuitry of module 65 may be comprised in one of the processor complexes of a parallel processor of the type described in the aforesaid copending applications, and the circuitry of the other module 67 may be comprised in an-

other processor complex of the parallel processor. The circuitry of the two modules 65, 67 may be connected together via an intercomplex network connection 70 that permits data from the one of the processor complexes 65 to be provided to the other processor complex 67.

5 One or more of the function blocks (i.e., function blocks A, B) 60, 62 of module 65 may comprise sequential logic circuits that may receive inputs 50, 80 from sources (not shown) external to the design 100 and externally-generated clock signals CLK. The blocks 60, 62 may generate and supply outputs based upon the inputs 50, 80 and clock signals CLK to downstream function block (i.e., function block X) 64 of the module 65.

10 Downstream block 64 may comprise combinatorial logic circuitry that further processes the outputs supplied to it by the block 60 to generate outputs that are supplied to the function block 66 (i.e., function block Y). Block 66 may comprise driver circuitry that drives the signals supplied to it from the block 64 onto connection 70 for reception by function block 72 (i.e., function block Z) of the other module 67. Block 72 may com-

15 prise receiver circuitry that processes the signals it receives from module 65 for use by function block 74 (i.e., function block C). Function block 74 may comprise sequential logic circuitry that processes the signals it receives from the block 72 based upon external signals CLK to produce outputs that are supplied to another sequential logic circuitry block (i.e., function block D) 76. Block 76 processes the signals that it receives from

20 block 74 based upon clock signals 76 to produce outputs 78. Function blocks 60, 62, 64 (i.e., function blocks A, B, X) typically may be much larger than function block 66 (i.e., function block Y).

Turning now to Figures 1 and 2, system 10 comprises a graphical user interface 20 that permits the user to graphically and/or textually input specifications of the proposed design 100. If textually-based, these specifications may be input directly by the user in the form of Verilog™ and/or Very High Level Hardware Descriptor (VHDL)-compatible statements (i.e., statements that may be compiled using conventional techniques into a Verilog™ and/or VHDL netlist description of the design 100). If graphically-based, these specifications may be input by the user in the form of graphical symbols and the like which may be converted by the interface 20 into Verilog™ and/or VHDL-compatible statements.

Regardless of whether they are input directly by the user in the form of Verilog™ and/or VHDL-compatible statements, or converted thereto by the interface 20, the statements are compiled by conventional netlist generator 22 into a complete Verilog™ and/or VHDL netlist description of the design 100. The netlist description generated by the generator 22 may be displayed by the user interface 20 for review and/or editing by the user via the interface 20. The netlist description is then provided by the generator 22 to physical characteristic modeling engine 24.

Using conventional techniques, engine 24 generates from the netlist description, physical data that provides a physically-accurate description of the design 100. More specifically, with reference to Figure 2, using conventional techniques, the physical placement/routing engine 40 of physical modeling engine 24 determines from the netlist description and predetermined physical design rules (e.g., preprogrammed into the engine 40 and/or provided by the user), the physical placement, compositions, construction, and layout of the design's circuit paths and electronic components (hereinafter referred to

collectively as the design's "physical layout") of the design 100. Using conventional techniques, the SPEF data generator 42 of engine 24 then computes from the design's physical layout the relevant physical characteristics (e.g., input and output impedances, capacitances, etc.) of all of the components, circuit traces, electrical connection lines, etc. of the design 100, based upon well-known physical laws that correlate these physical characteristics to the design's physical layout. Data indicative of these relevant physical characteristics may be generated by the generator 42 and stored in the database 46 in an industry standard data format (e.g., the Standard Parasitic Exchange Format, "SPEF"). Using conventional techniques and well-known physical laws, the SDF generator 44 in engine 24 then generates from the relevant physical characteristics the estimated signal propagation delays for signals transmitted through at least certain components, circuit traces, electrical connection lines in the design 100. Data indicative of these estimated propagation delays may be generated by the generator 44 and stored in the database 48 in an industry standard data format (e.g., the Standard Delay Format, "SDF").

In system 10, the SPEF and SDF data stored in databases 46, 48, respectively, of engine 24 are made available to both conventional HA modeling engine 28 and composite modeling engine 30. Conversely, in system 300, the engine 24' provides the data in databases 46, 48 to only engine 28, but otherwise operates in a manner that is substantially identical to engine 24 of system 10. Using conventional techniques, the HA modeling engine 28 uses the SPEF and SDF data, and the netlist description of the design 100 to generate an HA model 150 of the design 100. This HA model 150 is schematically illustrated in Figure 4.

As shown schematically in Figure 4, in the HA model 150 of design 100, functions 82, 84, and 86 are used. In essence, functions 82, 84, 86 are mathematical functional abstractions, based upon the physical characteristics of the proposed design 100 in the databases 46, 48, that may be used to estimate the overall timing operations of module 65, connection 70, and module 67, respectively, as a functions of the inputs 50, 80 and clock signals CLK provided thereto. More specifically, function 82 essentially is an approximate mathematical model of the overall timing operation of the module 65 that is based upon, but is not itself, an accurate description of the physical characteristics of the circuits, networks, etc. comprised in module 65 or blocks 60, 62, 64, and 66 comprised in module 65. Similarly, function 84 essentially is an approximate mathematical model of the overall timing operation of the connection 70 that is based upon, but is not itself, an accurate description of the physical characteristics of the connection 70. Also similarly, function 86 essentially is an approximate mathematical model of the overall timing operation of the module 67 that is based upon, but is not itself, an accurate description of the physical characteristics of the circuits, networks, etc. comprised in module 67 or blocks 72, 74, 76, comprised in module 67.

Before completing the description of system 10, we briefly return to describing the prior system 300, in order to point out the differences between system 10 and the prior art system 300. In prior art system 300 illustrated in Figure 6, the HA model 150 generated by engine 28 is supplied to a timing simulation engine 32', which simulates the timing operation of the design 100 based upon the HA model 150 and timing constraint commands supplied to engine 32' from the timing constraint generator 26. More specifically, the user may input and edit various timing constraints (e.g., the timing of clock sig-

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optionally, user-specified parameters provided by the user via interface 20. The parameters may specify, e.g., a portion of the design 100 (i.e., the function blocks and/or network connections) that is to be modeled using physical characteristics instead of HA models. Alternatively, the engine 30 may implement a process that uses empirically-determined hybrid modeling rules to select the portion or portions of the design 100 that are to be modeled by engine 30 using their physical characteristics rather than HA functions. The engine 30 modifies the HA model 150 generated by the engine 28 in accordance with the parameters, if provided by the user, or the process, and physical characteristics to generate a hybrid HA/physical characteristics-based model (e.g., model 200 illustrated schematically in Figure 5). This hybrid model 200 is provided to the timing simulation engine 32 which uses this model 200, instead of the HA model 150, and the timing constraint commands provided by generator 26 to calculate the simulated timing operation of the design 100. The results of these calculations may be provided to interface 20 which may graphically display them for analysis by the user.

More specifically, as shown in Figure 5, hybrid model 200 includes both estimated HA functions 90, 92 of portions of the design 100, and physically-accurate descriptions 92, 94, 96 (i.e., actual physical characteristics) of other portions of the design 100. That is, function 90 is an HA-based estimated function of the overall timing operation of the blocks 60, 62, 64 of the module 65. Function 92 is an HA-based estimated function of the overall timing operation of the blocks 74, 76 of the module 67. In hybrid model 200, the actual physical characteristics (e.g., as stored in the SPEF and SDF databases 46, 48) of the block 66, network connection 70, and block 72 are used along with these functions 90, 92 to permit the timing operation of the design 100 to be simulated

more accurately than is possible when such simulation is based upon HA-based model
150.

That is, in simulating the timing operation of the design 100, in addition to using
the timing constraint commands provided by the generator 26, the engine 32 uses the HA
5 function 90 to estimate the overall timing operation of the portion of the module 65 that
comprises blocks 60, 62, 64. Similarly, the engine 32 uses the HA function 92 to esti-
mate the overall timing operation of the portion of the module 67 that comprises blocks
74 and 76. However, the engine 32 calculates the respective timing operations of block
66, connection 70, and block 76 using the respective actual physically characteristics 92,
10 94, 96 of these components 66, 70, 76. In order to calculate the overall timing operation
of the design 100, the timing operations calculated using the functions 90, 92, and de-
scriptions 92, 94, 96 may be combined.

As noted above, the portions 66, 70, 72 of the design 100 that are modeled in
model 200 using their actual physical characteristics may be selected in accordance with
15 parameters supplied to the engine 30 from the user via the interface 20, or by a selection
process implemented by the engine 30. If the parameters are appropriately selected by
the user, the competing interests of minimizing the simulation's approximation error and
required processing overhead may be optimally balanced. That is, by appropriately se-
lecting parameters, the simulation's approximation error may be reduced to below a de-
20 sired threshold, without unduly increasing the amount of processing overhead needed to
generate the simulation to an undesirable level.

Alternatively, the engine 30 may implement a process that optimally selects the
portion of the design 100 that is to be modeled using physical characteristics instead of

HA functions. According to this process, the portion of design 100 that is to be modeled using physical characteristics is selected based upon empirically-determined simulation optimization rules that have been determined to maximize possibility of increasing accuracy of the simulation without unduly increasing the processing overhead required to generate the simulation. For example, as is often the case in designs such as design 100 that comprise an intermodule cross-chip connection 70, it has been empirically determined that optimal results in terms of maximizing accuracy of the simulation without unduly increasing the processing overhead required for the simulation tend to occur when the physical characteristics of connection 70 and function blocks (e.g., blocks 66 and 72) that are directly connected to the connection 70 are simulated using their physical characteristics instead of HA functions. Based upon this empirically-determined rule, the engine 30 may modify the model 150 by essentially "repartitioning" the boundaries of the HA functions such that blocks 60, 62, 64 in one module 65 that are not directly connected to the connection 70 are modeled using one HA function 90, blocks 74, 76 that are in the other module 67 and are also not directly connected to connection 70 are modeled using another HA function 92, and the blocks 92, 96 that are connected to connection 70, and connection 70 itself, are modeled using their physical characteristics 93, 94, 96. As will be appreciated, engine 30 may be programmed with additional empirically-determined optimization rules for optimally modifying other designs in accordance with this process.

Thus, it is evident that there has been provided, in accordance with the present invention, an electronic system modeling technique that fully satisfies the aims and objectives, and achieves the advantages set forth above. As will be apparent to those skilled in the art, many alternatives, modifications, and variations of the embodiments described

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What is claimed is: